



SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
COIMBATORE-35



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REGULATIONS -2023

SUGGESTED CURRICULUM

M.E – VLSI DESIGN

SEMESTER I									
S No.	Course Code	Course	L	T	P	Contact hrs/week	Credit	Int/Ext	Category
Theory Courses									
1.	23MAT605	Applied Mathematics for Electronics Engineers	3	1	0	4	4	40/60	FC
2.	23VLT601	Analog IC Design	3	0	0	3	3	40/60	PC
3.	23VLT602	Digital CMOS VLSI Design	3	0	0	3	3	40/60	PC
4.	23VLT603	ASIC and FPGA Design	3	0	0	3	3	40/60	PC
5.	23VLT604	Semiconductor Devices and Modeling	3	0	0	3	3	40/60	PC
6.	23VLEXXX	Professional Elective – I	3	0	0	3	3	40/60	PE
7.		Audit Course-I	2	0	0	2	-	-	
Theory Integrated Practical Courses									
8.	23GEB601	Design Thinking	1	0	4	5	3	50/50	EEC
Practical Courses									
9.	23VLP601	VLSI Design Laboratory-I	0	0	4	4	2	60/40	PC
Total			21	1	8	30	24		

SEMESTER II									
S No.	Course Code	Course	L	T	P	Contact hrs/week	Credit	Int/Ext	Category
Theory Courses									
1.	23VLT605	VLSI Signal Processing	3	0	0	3	3	40/60	PC
2.	23VLT606	RF IC Design	3	0	0	3	3	40/60	PC
3.	23VLT607	VLSI Testing	3	0	0	3	3	40/60	PC
4.	23VLEXXX	Professional Elective-II	3	0	0	3	3	40/60	PE
5.	23VLEXXX	Professional Elective-III	3	0	0	3	3	40/60	PE

6.		Audit Course-II	2	0	0	2	0	-	EEC
7.		Career course-I	2	0	0	2	2	40/60	EEC
Practical Courses									
8.	23VLP602	VLSI Design Laboratory-II	0	0	4	4	2	60/40	PC
Total			19	0	4	23	19		

SEMESTER III									
S No.	Course Code	Course	L	T	P	Contact hrs/week	Credit	Int/Ext	Category
Theory Courses									
1.	23VLEXXX	Professional Elective-IV	3	0	0	3	3	40/60	PE
2.	23VLEXXX	Professional Elective-V	3	0	0	3	3	40/60	PE
3.		Open Elective	3	0	0	3	3	40/60	OE
4.		Career Course II	2	0	0	2	2	40/60	EEC
Practical Courses									
5.	23VLP701	Project –I	0	0	12	12	6	60/40	EEC
Total			11	0	12	23	17		

SEMESTER IV									
S No.	Course Code	Course	L	T	P	Contact hrs/week	Credit	Int/Ext	Category
Practical Courses									
1.	23VLP702	Project –II	0	0	24	24	12	60/40	EEC
Total			0	0	24	24	12		

TOTAL CREDITS OF THE PROGRAMME: 72

FOUNDATION COURSE (FC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23MAT605	Applied Mathematics	4	3	1	0	4

PROFESSIONAL CORE (PC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23VLT601	Analog IC Design	3	3	0	0	3
2.	23VLT602	Digital CMOS VLSI Design	3	3	0	0	3
3.	23VLT603	ASIC and FPGA Design	3	3	0	0	3
4.	23VLT604	Semiconductor Devices and Modeling	3	3	0	0	3
5.	23VLT605	VLSI Signal Processing	3	3	0	0	3
6.	23VLT606	RF IC Design	3	3	0	0	3
7.	23VLT607	VLSI Testing	3	3	0	0	3
8.	23VLP601	VLSI Design Laboratory-I	4	0	0	4	2
9.	23VLP602	VLSI Design Laboratory-II	4	0	0	4	2

PROFESSIONAL ELECTIVES – (PE)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
PROFESSIONAL ELECTIVE I							
1.	23VLE601	Advanced Computer Architecture and Parallel Processing	3	3	0	0	3
2.	23VLE602	Electronic Packaging Technologies	3	3	0	0	3
3.	23VLE603	Hardware Security	3	3	0	0	3
4.	23VLE604	VLSI for IoT Systems	3	3	0	0	3
5.	23VLE605	Bio Medical Signal Processing	3	3	0	0	3
6.	23VLE606	Advanced Digital System Design	3	3	0	0	3

PROFESSIONAL ELECTIVE II							
7.	23VLE607	DSP Processors Architecture and Programming	3	3	0	0	3
8.	23VLE608	Physical Design of VLSI circuits	3	3	0	0	3
9.	23VLE609	Signal integrity for high speed devices	3	3	0	0	3
10.	23VLE610	CMOS Mixed Signal Circuit Design	3	3	0	0	3
11.	23VLE611	Genetic Algorithms for VLSI	3	3	0	0	3
12.	23VLE612	Advanced Wireless Sensor Networks	3	3	0	0	3
PROFESSIONAL ELECTIVE III							
13.	23VLE613	VLSI Architecture for Image and Video Processing	3	3	0	0	3
14.	23VLE614	Network on Chip	3	3	0	0	3
15.	23VLE615	CAD for VLSI Design	3	3	0	0	3
16.	23VLE616	Nanoscale Devices	3	3	0	0	3
17.	23VLE617	VLSI for Wireless Communication	3	3	0	0	3
18.	23VLE618	Power Efficient VLSI Design	3	3	0	0	3
PROFESSIONAL ELECTIVE IV							
19.	23VLE619	System Verilog	3	3	0	0	3
20.	23VLE620	Hardware Software Co-Design for FPGA	3	3	0	0	3
21.	23VLE621	Adaptive Signal Processing	3	3	0	0	3
22.	23VLE622	Design of Semiconductor memories	3	3	0	0	3
23.	23VLE623	Solar Photo Voltaic System	3	3	0	0	3
PROFESSIONAL ELECTIVE V							
24.	23VLE624	DSP Integrated Circuits	3	3	0	0	3
25.	23VLE625	Mixed Signal VLSI Design	3	3	0	0	3
26.	23VLE626	Reconfigurable Architectures	3	3	0	0	3

27.	23VLE627	Design for Verification using UVM	3	3	0	0	3
28.	23VLE628	Soft Computing and Optimization Techniques	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23GEB601	Design Thinking	5	1	0	4	3
2.	23VLP701	Project – I	12	0	0	12	6
3.	23VLP702	Project - II	24	0	0	24	12
4.		Audit Course-I	2	2	0	0	-
5.		Audit Course-II	2	2	0	0	-
6.		Career Course I	2	2	0	0	2
7.		Career Course II	2	2	0	0	2

OPEN ELECTIVE OFFERED TO OTHER PROGRAMMES

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23VLO701	System On Chip	3	3	0	0	3
2.	23VLO702	VLSI Design Techniques	3	3	0	0	3
3.	23VLO703	VLSI Technology	3	3	0	0	3
4.	23VLO704	MEMS and its Applications	3	3	0	0	3

CAREER COURSE

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23GET601	Professional Development	2	2	0	0	2
2.	23GET602	Quality Assurance in Engineering Education	2	2	0	0	2
3.	23GET603	Holistic Education	2	2	0	0	2

AUDIT COURSE

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C
1.	23GEA601	English for Research Paper Writing	2	2	0	0	0
2.	23GEA602	Disaster Management	2	2	0	0	0
3.	23GEA603	Value Education	2	2	0	0	0
4.	23GEA604	Constitution of India	2	2	0	0	0
5.	23GEA605	Pedagogy Studies	2	2	0	0	0
6.	23GEA606	Sustainable Career Development	2	2	0	0	0

S.No.	SUBJECT AREA	Credits Per Semester				Total Credits
		I	II	III	IV	
1	FC	4	-	-	-	4
2	PC	14	11	-	-	25
3	PE	3	6	6	-	15
4	OE	-	-	3	-	3
5	EEC	3	2	8	12	25
TOTAL CREDITS		24	19	17	12	72

SEMESTER -I
FOUNDATION COURSE

23MAT605	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C	
		3	1	0	4	
COURSE OBJECTIVES :						
<ul style="list-style-type: none"> ● To demonstrate various analytical skills in applied mathematics. ● To study performance of probability, dynamic programming and queuing theory. 						
UNIT I	FUZZY LOGIC					9+3
Classical logic – Multi valued logics – Fuzzy propositions – Fuzzy quantifiers.						
UNIT II	MATRIX THEORY					9+3
Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications.						
UNIT III	ONE DIMENSIONAL RANDOM VARIABLES					9+3
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.						
UNIT IV	DYNAMIC PROGRAMMING					9+3
Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.						
UNIT V	QUEUEING MODELS					9+3
Poisson Process – Markovian queues – Single and Multi-server Models – Little’s formula - Machine Interference Model – Steady State analysis – Self Service queue.						
		L : 45	T:15	P: 0	Total: 60 PERIODS	
REFERENCES						
1	George.J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 2011.					
2	Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.					
3	Johnson, R.A., Miller, I and Freund J., "Miller and Freund"s Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.					
4	Taha, H.A. Operations Research: An Introduction, Ninth Edition, Pearson Education Edition, Asia, New Delhi, 2016.					
5	Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queuing Theory", 4th Edition, John Wiley, 2014					
COURSE OUTCOMES						
At the end of the course student should be able to:						
CO1	Select the concept of fuzzy sets, knowledge representation using fuzzy rules.					
CO2	Know how to compute certain matrix decompositions and some of their applications.					

C03	Associate the Computation of probability and moments with standard distributions.
C04	Infer the Mathematical areas in Dynamic Programming.
C05	Estimate the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3	3	2									2	
C02	3	3	2									2	
C03	3	3	2									2	
C04	3	3	2									2	
C05	3	3	2									2	

PROFESSIONAL CORE (PC)

23VLT601	ANALOG IC DESIGN	L	T	P	C	
		3	0	0	3	
COURSE OBJECTIVES :						
<ul style="list-style-type: none"> • To get familiar with the MOSFET structure, Operation, and modeling. • To learn and analyse the Single stage Amplifiers, Differential Amplifier, Operational Amplifier and understand the concepts of stability and frequency compensation. 						
UNIT I	MOSFET METRICS					9
Basic MOS physics and equivalent circuits -MOS IV Characteristics-Simple long channel MOSFET Theory- Technology trend, Need for Analog design -Sub- micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub- threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller's approximation.						
UNIT II	SINGLE STAGE AMPLIFIERS					9
Single stage Amplifiers-CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.						
UNIT III	FEEDBACK AND OPERATIONAL AMPLIFIERS					9
Properties and types of negative feedback circuits, effect of loading in feedback networks Performance metrics-Single stage OPAMP-Double stage OPAMP-Gain Boosting-Comparison- Output Swing Calculation-Common mode Feedback-Input range limitation-Slewrate-High slewrate OPAMPs-Power Supply rejection.						
UNIT IV	STABILITY AND FREQUENCY COMPENSATION					9
Basic Concepts, Instability and the Nyquist Criterion.Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of two stage OP Amps.						
UNIT V	BANDGAP REFERENCES					9
Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.						
		L : 45	T:0	P: 0	Total: 45 PERIODS	
REFERENCES						
1	Behzad Razavi, "Design Of Analog Cmos Integrated Circuits", Tata Mcgraw Hill, 2017.					
2	Willey M.C. Sansen, "Analog Design Essentials", Springer, 2017.					
3	Grebene, "Bipolar And Mos Analog Integrated Circuit Design", John Wiley & Sons,Inc.,2003.					
4	Phillip E.Allen, Douglas R .Holberg, "Cmos Analog Circuit Design", Oxford University Press, 3 rd Edition, 2016.					
5	Jacob Baker "CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3 rd					

	Edition, 2010.
COURSE OUTCOMES	
At the end of the course student should be able to:	
C01	Summarise the characteristics and models of MOS devices
C02	Design amplifiers to meet user specifications
C03	Design and analyse feedback amplifiers and one stage op amps
C04	Understand stability analysis and frequency compensation techniques of amplifiers.
C05	Design and analyse current mirrors and current sinks with mos devices

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3			3	3							3	
C02		3	3		3				3				
C03		3	3	3									
C04	3												
C05		3	3	3	3							3	

23VLT602	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES :

- To learn the fundamental principles of VLSI circuit design in digital domain and understand design methodology of arithmetic building block and memory architecture
- To Understand and apply interconnect and clocking strategy

UNIT I	MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	9
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MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II	COMBINATIONAL LOGIC CIRCUITS	9
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Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore"s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III	SEQUENTIAL LOGIC CIRCUITS	9
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Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non-bistable Sequential Circuits.

UNIT IV	ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES	9
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Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V	INTERCONNECT AND CLOCKING STRATEGIES	9
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Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

L : 45	T:0	P: 0	Total: 45 PERIODS
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REFERENCES

1	Jan Rabaey, Anantha Chandrakasan, B Nikolic, 'Digital Integrated Circuits: A Design Perspective'. Second Edition, Prentice Hall of India., 2009.
2	Jacob Baker, 'CMOS: Circuit Design, Layout, and Simulation', Third Edition, Wiley IEEE Press, 2011
3	M J Smith, 'Application Specific Integrated Circuits', Addison Wesley, 1997.
4	N.Weste, K. Eshraghian, 'Principles of CMOS VLSI Design'. Second Edition, Addison Wesley, 1993.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1	Familiarize the static and dynamic characteristic of MOSFET and its parameters.
CO2	Understand the concepts of combinational logic circuits with layout design rules.
CO3	Analyze the sequential logic circuits and its clock and timing issues
CO4	Interpret the nature of datapath circuits in arithmetic circuits and memory devices.
CO5	Estimate the clocking strategies used for designing synchronous circuit design

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3			3	3							3	
C02	3				3							3	
C03		3	3	3	3							3	
C04		3	3	3	3								
C05	3	3	3		3								

23VLT603	ASIC AND FPGA DESIGN			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES :							
<ul style="list-style-type: none"> To prepare the student to be an entry-level industrial standard ASIC or FPGA designer. To understand the of basics of Silicon on Chip. 							
UNIT I	INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN						9
Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture.							
UNIT II	PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS						9
Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Xilinx I/O blocks.							
UNIT III	PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY						9
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.							
UNIT IV	SILICON ON CHIP DESIGN						9
Voice over IP SOC - Intellectual Property – SOC Design challenges- Methodology and design- FPGA to ASIC conversion – Design for integration-SOC verification -Set top box SOC							
UNIT V	PHYSICAL AND LOW POWER DESIGN						9
Over view of physical design flow- tips and guideline for physical design- modern physical design techniques- power dissipation-low power design techniques and methodologies-low power design tools- tips and guideline for low power design.							
				L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES							
1	M.J.S. Smith, Application Specific Integrated Circuits, Pearson Education, 2008.						
2	FarzadNekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.						
3	Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2009.						
4	Rajsuman, System-on-a-Chip Design and Test, Santa Clara, CA: Artech House Publishers, 2000.						
5	F.Nekoogar, Timing Verification of Application-Specific Integrated Circuits (ASICs), Prentice Hall PTR, 1999.						
COURSE OUTCOMES							
At the end of the course student should be able to:							
CO1	Classify the types of ASICs and the ASIC library design.						
CO2	Relate the PROM technologies in Xilinx and Altera FPGA market.						

C03	Understand the concepts of ASIC interconnects and software used in PLA design
C04	Evaluate the SOC design challenges and design for integration in applications.
C05	Model a low power circuit with satisfied physical design

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3			3	3							3	
C02	3			3	3							3	
C03	3			3	3							3	
C04		3	3	3	3					3		3	
C05		3	3	3	3					3		3	

23VLT604	SEMICONDUCTOR DEVICES AND MODELING				L	T	P	C
		3	0	0	3			
COURSE OBJECTIVES :								
<ul style="list-style-type: none"> To study the operation and modeling of the MOS Capacitor and MOSFETs To learn the device level characteristics of BJT transistors and the suitable mathematical technique for simulation. 								
UNIT I	MOS CAPACITORS							9
Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon-Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide								
UNIT II	MOSFET DEVICES							9
Long-Channel MOSFETs, Drain-Current Model, MOSFET I-V Characteristics, Subthreshold Characteristics, Substrate Bias, and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, MOSFET Degradation and Breakdown at High Fields.								
UNIT III	CMOS DEVICE DESIGN							9
CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C-V Measurements.								
UNIT IV	BIPOLAR DEVICES							9
n-p-n Transistors, Basic Operation of a Bipolar Transistor, Ideal Current-Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC-VCE Characteristics, Characteristics of a Typical n-p-n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base-Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base-Collector Junction Avalanche, Saturation Currents in a Transistor.								
UNIT V	MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS							9
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.								
					L : 45	T:0	P: 0	Total: 45 PERIODS

REFERENCES	
1	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2021.
2	A.B. Bhattacharyya "Compact MOSFET Models for VLSI Design", John Wiley & Sons Ltd, 2009.
3	Ansgar Jungel, "Transport Equations for Semiconductors", Springer, 2009
4	Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 2011.
5	Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 2nd Edition, 2014

COURSE OUTCOMES	
At the end of the course student should be able to:	
CO1	Explore the properties of MOS capacitors.
CO2	Analyze the various characteristics of MOSFET devices.
CO3	Describe the various CMOS design parameters and their impact on performance of the device.
CO4	Discuss the device level characteristics of BJT transistors.
CO5	Identify the suitable mathematical technique for simulation.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3			3								3	
CO2		3	3	3								3	
CO3	3			3								3	
CO4	3			3								3	
CO5		3	3	3	3							3	

23VLP601	VLSI DESIGN LABORATORY-I	L	T	P	C
		0	0	4	2
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To learn the HDL codes for adder Circuits,multipliers and filter design To understand the HDL codes for ALU and Display circuit design ,Comparators and Counters and I/O interfacing using FPGA 					
LIST OF EXPERIMENTS					
<ol style="list-style-type: none"> Design of 8-bit Carry Skip Adder and Carry Save Adder Design of 4-bit Array Multiplier and with and without Pipelining Design of 4-tap FIR Filter with and without Pipelining Design of 8-bit ALU Design and implementation of seven segment display Design of Comparator Design of Synchronous up counter and down counter FPGA Real time Programming and I/O Interfacing Interfacing with memory modules in FPGA Boards Introduction to Cadence. 					
MAJOR EQUIPMENTS / SOFTWARE REQUIRED					
<ul style="list-style-type: none"> Ram : 16 GB Processor : i5 Operating system : Windows , Linux Software : Xilinx ISE 10.1,Cadence tool Hardware : Xilinx FPGA Spartan Kits 					
L : 0		T : 0	P: 60	C: 2	Total:60 PERIODS
COURSE OUTCOMES					
At the end of the course student should be able to:					
C01	Develop HDL codes for adder Circuits				
C02	Build HDL codes for multipliers and filter design				
C03	Examine the HDL codes for ALU and Display circuit design				
C04	Simulate the HDL codes for Comparators and Counters				
C05	Develop a real time program for I/O interfacing using FPGA				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3	3	3		3		3					3	3
C02	3		3	3	3		3					3	3
C03	3	3	3		3		3					3	3
C04	3	3	3	3	3		3					3	3
C05	3	3	3	3	3		3					3	3

SEMESTER II

23VLT605	VLSI SIGNAL PROCESSING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> • To introduce techniques for altering existing DSP structures to suit VLSI implementations. • To introduce efficient design of DSP architectures suitable for VLSI. 					
UNIT I	PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS	9			
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.					
UNIT II	ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I	9			
Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.					
UNIT III	ALGORITHMIC STRENGTH REDUCTION -II	9			
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.					
UNIT IV	BIT-LEVEL ARITHMETIC ARCHITECTURES	9			
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.					
UNIT V	NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING	9			
Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.					
		L:45	T: 0	P:0	Total: 45 PERIODS
REFERENCES					
1	Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and implementation “, Wiley, Interscience, 2007.				
2	U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2014.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Familiarize the pipelining an parallel processing of filters in VLSI circuits.				
CO2	Analyze the algorithmic strength reduction techniques in FIR filters.				
CO3	Analyze the algorithmic strength reduction techniques in IIR filters.				
CO4	Understand the basic concepts of bit level arithmetic architectures.				

C05	Estimate the strength reduction, clocking and pipelining approaches in VLSI Processors
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COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3		3		3							3	3
C02	3	3	3		3							3	
C03	3	3	3		3							3	
C04	3		3		3							3	3
C05	3	3	3		3							3	3

23VLT606	RF IC DESIGN			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES :							
<ul style="list-style-type: none"> To study the various impedance matching techniques used in RF circuit design. To understand the functional design aspects of LNAs, Mixers, PLLs , VCOs and Frequency synthesizers. 							
UNIT I	IMPEDANCE MATCHING IN AMPLIFIERS						9
Circuit basics for RF design , Definition of 'Q', Series Parallel Transformations of Lossy Circuits, Impedance Matching Using 'L','Pi' and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers, Duplexing, FDMA.							
UNIT II	AMPLIFIER DESIGN						9
Noise Characteristics of MOS Devices, Review of MOSFET, RF transistor layout, Design of CG LNA and Inductor Degenerated LNAs, Principles of RF Power Amplifiers Design, Basic Heterodyne and Homodynes architecture.							
UNIT III	ACTIVE AND PASSIVE MIXERS						9
Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise, Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.							
UNIT IV	OSCILLATORS						9
LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise, Low-noise VCO topologies.							
UNIT V	PLL AND FREQUENCY SYNTHESIZERS						9
Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer, 5G and WiFi circuits and systems							
				L:45	T: 0	P: 0	Total: 45 PERIODS
REFERENCES							
1	B.Razavi ,”RF Microelectronics” , Prentice-Hall ,2nd Edition,2011.						
2	Bosco H Leung “VLSI for WirelessCommunication”,PearsonEducation,2nd Edition,2014						
3	Behzad Razavi, “Design of Analog CMOS Integrated Circuits” Mcgraw-Hill, 2nd Edition,2017.						
4	Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2011						
5	Thomas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits’, Cambridge University Press ,2003.						
COURSE OUTCOMES							
At the end of the course student should be able to:							
CO1	Understand the principles of operation of an RF receiver front end.						
CO2	Apply constraints for LNAs, Mixers and frequency synthesizers.						
CO3	Analyze and design mixers.						

C04	Design different types of oscillators and perform noise analysis.
C05	Design PLL and frequency synthesizer.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3		3		3							3	3
C02	3	3	3	3	3							3	3
C03	3	3	3	3	3							3	3
C04	3	3	3	3	3							3	3
C05	3	3	3	3	3							3	3

23VLT607	VLSI TESTING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES:					
<ul style="list-style-type: none"> To Introduce the VLSI testing, logic and fault simulation and testability measures To Study the test generation for combinational and sequential circuits, design for testability and fault diagnosis. 					
UNIT I	BASICS OF TESTING AND FAULT MODELING	9			
Introduction to testing – Faults in Digital Circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.- Check point Theorem.					
UNIT II	TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	9			
Test generation for combinational logic circuits – Testable combinational logic circuit design – ATPG for Combinational Circuits -Test generation for sequential circuits – design of testable sequential circuits.					
UNIT III	DESIGN FOR TESTABILITY	9			
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches, Chip level testing.					
UNIT IV	SELF – TEST AND TEST ALGORITHMS	9			
Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs- D-algorithm- PODEM Algorithm- FAN Algorithm					
UNIT V	FAULT DIAGNOSIS	9			
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis. Fault Diagnosis in Sequential Circuits Introduction to programmable logic devices: PALs, PLDs, CPLDs and FPGAs.					
		L:45	T: 0	P: 0	Total: 45 PERIODS
REFERENCES					
1	M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.				
2	P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.				
3	M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2004.				
4	A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Understand the basic concepts of fault modeling and detection in digital circuits.				
CO2	Familiarize the methods of test generation by combinational and sequential logic circuits.				
CO3	Infer the concept of DFT by various scan based approaches.				
CO4	Estimate the faulty circuits using BIST architectures by test algorithms.				
CO5	Analyze the digital circuits using logic and system level diagnostics.				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3		3		3							3	
C02	3	3	3	3	3							3	
C03	3	3	3	3	3							3	3
C04	3	3	3	3	3							3	3
C05	3	3	3	3	3							3	3

23VLP602	VLSI DESIGN LABORATORY-II	L	T	P	C	
		0	0	4	2	
COURSE OBJECTIVES:						
<ul style="list-style-type: none"> Understand the design and operation of basic analog circuits Develop proficiency in designing complex analog circuits 						
LIST OF EXPERIMENTS						
	<ol style="list-style-type: none"> Design of Common source amplifier with different loads Design of Common gate amplifier Design of Common drain amplifier Design of Single stage cascode amplifier Design of Current mirror Design of differential amplifier with different loads Design of two stage OPAMP Design of telescopic cascade OPAMP Fault detection and diagnosis for combinational circuits Fault detection and diagnosis for sequential circuits 					
MAJOR EQUIPMENTS / SOFTWARE REQUIRED						
	<ul style="list-style-type: none"> Ram : 16 GB Processor : i5 Operating system : Linux Software : Xilinx ,Cadence tool 					
		L : 0	T: 0	P: 60	C: 2	Total:60 PERIODS
COURSE OUTCOMES						
At the end of the course student should be able to:						
C01	Design Analog integrated circuits taking account the parasitic effects.					
C02	Simulate the Analog integrated circuits using cadence tool.					
C03	Generate the layout of various analog Integrated circuits.					
C04	Analyze the operation and behavior of various analog integrated circuits.					
C05	Detect and Diagnose faults in combinational and sequential circuits.					

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3	3	3		3							3	3
C02	3		3	3	3							3	3
C03	3	3	3		3							3	3
C04	3	3	3	3	3							3	3
C05	3	3	3	3	3							3	3

PROFESSIONAL ELECTIVES (PE)

PROFESSIONAL ELECTIVE I

23VLE601	ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES:					
<p>The objective of this course are,</p> <ul style="list-style-type: none"> • To Explore parallel processing mechanisms. • To organize Memory and I/O subsystem and analyse pipelines and vectorization methods. 					
UNIT I	PARALLEL PROCESSING MECHANISMS	9			
Evolution of computer systems. Generation of computer systems– Trends towards parallel processing- Parallel processing mechanisms- parallel computer structure- Architectural classification schemes.					
UNIT II	MEMORY	9			
Memory and I/O subsystems: Hierarchical Memory structure – Virtual memory system - cache memory management- Memory allocation and management – I/O subsystems.					
UNIT III	PIPELINING	9			
Principles - Classification of pipeline processors - Reservation tables – Interleaved memory organization – Design of arithmetic pipeline – Design of instruction pipeline. Vector Processing: Need – Basic vector processing architecture - Issues in vector processing – Vectorization and optimization methods.					
UNIT IV	ARRAY PROCESSING	9			
SIMD Array processors – SIMD interconnection networks – Parallel algorithms for array processors – associative array processing .principles of parallel algorithm design: Design approaches-Design issues- Performance measures and analysis-Complexities-Anomalies in parallel algorithms.					
UNIT V	MULTIPROCESSOR ARCHITECTURE	9			
Functional structures - Interconnection network – Multi cache problems and solutions– Exploiting concurrency for multiprocessing. Network Computing: Client/Server Systems-clusters.					
		L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES					
1	Kai Hwang, Naresh Jotwani: Advanced Computer Architecture - Parallelism, Scalability, Programmability, Tata McGraw Hill,3 rd Edition,2017.				
2	John L Hennessy, “Computer Architecture a Quantitative Approach”, Harcourt Asia Pvt. Ltd., 2011.				
3	Seyed Roosta, “Parallel Processing and Parallel Algorithms”, Springer Series, 2000				
4	Hesham El-Rewini, Mostafa Abd-El-Barr, “Advanced Computer Architecture And Parallel Processing”, John Wiley & Sons, 2005.				

COURSE OUTCOMES	
At the end of the course student should be able to:	
C01	Explore parallel processing mechanisms.
C02	Analyse Memory and I/O subsystem organizations.
C03	Design and analyze pipelines and vectorization methods.
C04	Illustrate array processing architectures and design parallel algorithms
C05	Develop multiprocessor architectures and analyze their complexities.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3		1				2					1	2
C02	3	2	3	2	2		2				2	2	2
C03	3	2	3	2	2		3			2		2	2
C04	2	3	2	2	2	2	3		2			2	2
C05	2	1	3	2	2	2	2		2			3	2

23VLE602	ELECTRONIC PACKAGING TECHNOLOGIES	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To Brief the trends and levels of electronic systems packaging. To Analyze the commonly used and advanced packaging technologies. 					
UNIT I	OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING	9			
Packaged Electronics – Technologies- Trends- Products and levels of packaging- Packaging aspects of handheld products.					
UNIT II	SEMICONDUCTOR PACKAGING	9			
Basics of Semiconductor and Process flowchart; Wafer packaging; Packaging evolution- Chip connection choices -Wire bonding, TAB and flipchip. Single chip packages or modules (SCM).					
UNIT III	COMMONLY USED PACKAGES AND ADVANCED PACKAGING	9			
Commonly used packages and advanced packages; Materials in packages- Advanced packages - Thermal mismatch in packages; Current trends in packaging- Multichip modules (MCM)-types; System-in package(SIP)- Packaging roadmaps- Hybrid circuits.					
UNIT IV	ELECTRICAL DESIGN CONSIDERATIONS IN SYSTEMS PACKAGING	9			
Electrical Issues – Resistive Parasitic - Capacitive and Inductive Parasitic- Layout guidelines and the Reflection problem-Interconnection.					
UNIT V	THERMAL MANAGEMENT AND RELIABILITY	9			
Heat-transfer fundamentals-. Thermal conductivity and resistance- Conduction, convection and radiation- Cooling –Reliability- Basic concepts- Environmental interactions- Thermal mismatch and fatigue.					
L : 45		T:0	P: 0	Total: 45 PERIODS	
REFERENCES					
1	Rao R Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.				
2	William D Brown, “Advanced Electronic Packaging”, IEEE Press, 2006.				
3	Tummala, Rao R, “Microelectronics Packaging Handbook”, McGraw Hill, 2008.				
4	R.G.Kaduskar and V.B.Baru, “Electronic Product Design”, Wiley India, 2011.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Brief the trends and levels of electronic systems packaging.				
CO2	Analyze the commonly used and advanced packaging technologies.				
CO3	Identify the electrical design considerations in systems packaging.				
CO4	Identify the Commonly used packages and advanced packages.				
CO5	Illustrate the thermal management and reliability issues in packaging.				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3	2	3	2								1	2
C02	3	2	3	2	2						2	2	2
C03	3	2	3	2	2		2			2		2	2
C04	2	3	2	2	2	2	2		2			2	2
C05	2	3	3	2	2	2	2		2			3	1

23VLE603	HARDWARE SECURITY			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To Develop the various cryptographic algorithm implementations in hardware and explore the attacks. To Develop the various countermeasures using side channel analysis 							
UNIT I	CRYPTOGRAPHIC ALGORITHMS IMPLEMENTATION						9
Introduction - Need for hardware security – Basics and vulnerabilities - Design for security - Hardware Implementation of Public-key Cryptographic Algorithm - Private-key Cryptographic Algorithm - Stream Ciphers - Hash Functions.							
UNIT II	SIDE CHANNEL ANALYSIS						9
Introduction to Side Channel Analysis - Power Analysis Attack - Timing Attack - Fault Attack - Cache Attack – Scan Chain Based Attack - Design Techniques To Prevent Side Channel Analysis Attacks.							
UNIT III	HARDWARE TROJANS						9
Overview - Nomenclature and Operating Modes - Hardware Trojan Detection Techniques - Logic Testing - Countermeasures - Design Technique - Manufacturing Technique.							
UNIT IV	PHYSICALLY UNCLONABLE FUNCTIONS						9
Introduction – Design Approaches - Modeling of PUFs - Sources of Mismatch and Errors - Testing of PUFs - Practical Realizations - Applications.							
UNIT V	COUNTERFEIT ICS						9
Taxonomies - Assessment - Challenges - Detection and Prevention of Recycled ICs - Path Delay Fingerprinting – Secure Hardware Intellectual Properties: - Need for IP protection - Digital Watermarking - Constraint-based Watermarking to Design IP Protection - Watermarking HDL Source Codes by Duplicating Modules.							
				L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES							
1	Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design, Threats, and Safeguards", CRC Press, 2015.						
2	Mohammad Tehranipoor, Hassan Salmani, Xuehui Zhang, "Integrated Circuit Authentication Hardware Trojans and Counterfeit Detection", Springer, 2014.						
3	Christoph Bohm, Maximilian Hofer, "Physical Unclonable Functions in Theory and Practice", Springer, 2013						
4	Mohammad Tehranipoor, Cliff Wang, "Introduction to Hardware Security and Trust", Springer, 2012.						

5	Koc K C, "Cryptographic Engineering", Springer, 2009.
COURSE OUTCOMES	
At the end of the course student should be able to:	
C01	Develop the various cryptographic algorithm implementations in hardware and explore the attacks.
C02	Develop the various countermeasures using side channel analysis.
C03	Describe the effects of hardware trojans and methods to mitigate them.
C04	Model and test physically unclonable functions.
C05	Analyze the effects of counterfeiting ICs, mitigation methods and examine the various Intellectual Property (IP) protection techniques.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3		1									1	2
C02	3	2	3	2	2						2	2	2
C03	3	2	3	3	2		2			2		2	2
C04	2	3	2	3	2	3	2		2			2	2
C05	2	1	3	2	2	3	2		2			3	1

23VLE604	VLSI FOR IOT SYSTEMS			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To Describe the IoT framework and explore the modelling and design. To Explore the modelling validation of systems for variety of applications in IoT space and Design power optimized IoT system. 							
UNIT I	INTRODUCTION						9
Concept of connected world – Need, Legacy systems for connected world – features and limitations, Key features of IoT architecture, Merits and Demerits of IoT technology, Applications driven by IoT technology – examples.							
UNIT II	COMPONENTS OF IOT						9
Review of classic embedded system architecture, Basic building blocks of an IoT system –Sensors, Actuators, Computing nodes and Connectivity. Sensors used in IoT systems – Characteristics and requirements, Types of sensors for IoT systems, Compute nodes of IoT, Connectivity technologies in IoT – Software in IoT systems- Embedded Programming.							
UNIT III	IC TECHNOLOGY FOR IOT						9
SoC architecture for IoT Devices– Application Processors, Microcontrollers, Smart Analog; Memory architecture for IoT – Non Volatile Memories (NVM), Embedded Non-Volatile Memories, Anti-Fuse One Time Programmable (OTP) memories.							
UNIT IV	IC TECHNOLOGY POWER MANAGEMENT						9
Power Management - Low Drop Out Regulators, DC-to-DC Converters, Voltage References, Power Management Units (PMUs) in IC's and Systems, FPGA in IoT systems.							
UNIT V	ELECTRONIC SYSTEM DESIGN FOR IOT						9
Requirements, Designing Computing blocks in IoT systems. System Power Supply Design for IoT systems, Mixed Signal challenges in hardware systems, Form Factor – Guidelines and prevailing standards. Component models & System Design – Feasibility and challenges, System Level Integration, Operating conditions of IoT devices and impact on Electronic System Design; Hardware Security issues, EMI/EMC, SI/PI and Reliability Analysis in IoT systems.							
				L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES							
1	Alioto, "Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, First Edition, 2017.						
2	Pieter Harpe, Kofi A. A. Makinwa, Andrea Baschiroto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design", Springer International Publishing AG, 2017.						
3	Jim Lipman, Sidense Corp." NVM memory: A Critical Design Consideration for IoT Applications"- https://www.design-reuse.com/articles/32614/nvm-memory-iot-						

	applications.html.
4	ApekMulay, "Sustaining Moore's Law: Uncertainty Leading to a Certainty of IoT Revolution" Morgan and Claypool Publishers, 2015.
5	Rashid Khan, Kajari Ghoshdastidar, Ajith Vasudevan, "Learning IoT with Particle Photon and Electron", Packt Publishing Limited (Verlag), 2016.

COURSE OUTCOMES

At the end of the course student should be able to:

C01	Describe the IoT framework.
C02	Distinguish the features of IoT based systems.
C03	Explore the modelling and design.
C04	Explore the modelling validation of systems for variety of applications in IoT space.
C05	Design power optimized IoT system.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3	2	2	2								1	2
C02	3	2	3	2	2						2	2	2
C03	3	2	3	2	2		2			2		2	2
C04	2	3	2	2	2	3	2		2			2	2
C05	2	2	3	2	2	3	2		2			3	1

23VLE605	BIO MEDICAL SIGNAL PROCESSING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To understand concepts of signal processing and apply algorithms for signal processing. To analyse biomedical signals and systems. 					
UNIT I	INTRODUCTION TO BIOMEDICAL SIGNALS	9			
Action Potential and Its Generation, Origin and Waveform Characteristics of Basic Biomedical Signals Like: Electrocardiogram (ECG), Electroencephalogram (EEG), Electromyogram (EMG), Phonocardiogram (PCG), Electroneurogram (ENG), Event-Related Potentials (ERPS), Electrogastragram (EGG), Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Computer-Aided Diagnosis.					
UNIT II	REMOVAL OF NOISE AND ARTIFACTS FROM BIOMEDICAL SIGNAL	9			
Random and Structured Noise, Physiological Interference, Stationary and Nonstationary Processes, Noises and Artifacts Present in ECG, Time and Frequency Domain Filtering.					
UNIT III	EEG SIGNAL PROCESSING	9			
EEG Signal and Its Characteristics, EEG Analysis, Linear Prediction Theory, Autoregressive Method, Sleep EEG, Application of Adaptive Filter for Noise Cancellation in ECG and EEG Signals.					
UNIT IV	EVENT DETECTION IN BIOMEDICAL SIGNALS	9			
Detection of P, Q, R, S and T Waves in ECG, EEG Rhythms, Waves and Transients, Detection of Waves and Transients, Correlation Analysis Ad Coherence Analysis of EEG Channels.					
UNIT V	ANALYSIS OF NONSTATIONARY SIGNALS	9			
Heart Sounds and Murmurs, Characterization of Nonstationary Signals and Dynamic Systems, Short-Time Fourier Transform, Considerations in Short-Time Analysis and Adaptive Segmentation.					
		L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES					
1	Rangayyan, R.M., 2015. Biomedical signal analysis (Vol. 33). John Wiley & Sons, 2015.				
2	Reddy, D.C., Biomedical signal processing: principles and techniques. McGraw-Hill, 2005.				
3	Tompkins, W.J., Biomedical digital signal processing. Editorial Prentice Hall, 1998.				
4	Sörnmo, L. and Laguna, P., Bioelectrical signal processing in cardiac and neurological applications (Vol. 8). Academic Press, 2005.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Understand concepts of signal processing.				
CO2	Apply algorithms for signal processing.				
CO3	Analyse biomedical signals and systems.				
CO4	Evaluate biomedical signal processing systems.				
CO5	Evaluate nonstationary signals.				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes (1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3		1									2	3
C02	3	2	2	2	2						2	2	2
C03	3	2	2	2	2		2			2		2	2
C04	3	3	2	2	2	3	2		2			2	2
C05	3	2	3	2	2	3	2		2			3	2

23VLE606	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES :

- To understand the concepts of sequential circuits and its modeling techniques.
- To Apply the system design of digital circuits using VHDL programming.

UNIT I	SEQUENTIAL CIRCUIT DESIGN	9
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Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuit- design of iterative circuits-ASM chart and realization using ASM.

UNIT II	ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	9
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Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT III	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS	9
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Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT IV	SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES	9
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Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

UNIT V	SYSTEM DESIGN USING VHDL	9
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VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

L : 45 | T:0 | P: 0 | Total: 45 PERIODS

REFERENCES

1	Charles H.RothJr “Fundamentals of Logic Design” Thomson Learning,7 th Edition, 2013.
2	Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
3	ParagK.Lala “Fault Tolerant and Fault Testable Hardware Design” BS Publications,2002.
4	Parag K.Lala “Digital system Design using PLD” B S Publications,2003.
5	Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1	Understand the concepts of sequential circuits and its modeling techniques
CO2	Analyze the asynchronous circuit design and types of hazards in circuit design.
CO3	Familiarize the algorithmic methods used for fault diagnosing and testing in digital

	circuits
C04	Infer the families of PLDs and its types with applications.
C05	Apply the system design of digital circuits using VHDL programming.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	2												
C02	3			2	3							2	
C03	3			3	3								
C04	2											2	
C05	3					3							

PROFESSIONAL ELECTIVE II

23VLE607	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> • To Understand the fundamental concepts of various programmable DSPs. • To compare the performance of various advanced DSP and applications. 					
UNIT I	FUNDAMENTALS OF PROGRAMMABLE DSPs	9			
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs– Multiple access memory – Multi-port memory – VLIW architecture- Pipelining –Special Addressing modes in P-DSPs – On chip Peripherals.					
UNIT II	TMS320C5X PROCESSOR	9			
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Simple programs-Application Programs for processing real time signals.					
UNIT III	TMS320C3X PROCESSOR	9			
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.					
UNIT IV	ADSP PROCESSORS	9			
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.					
UNIT V	ADVANCED PROCESSORS	9			
Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.					
L : 45		T:0	P: 0	Total: 45 PERIODS	
REFERENCES					
1	B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.				
2	Sen M. Kuo, Woon-Seng Gan, ”Digital Signal Processors: Architectures, Implementations, and Applications”, Pearson, 2004				
3	Phil Lapsley, Jeff Bier, Amit Shoham, and Edward A. Lee, ”DSP Processor Fundamentals: Architectures and Features”, Wiley, 2004				
4	User guides Texas Instrumentation, Analog Devices, Motorola.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Understand the fundamental concepts of various programmable DSPs.				
CO2	Infer the characteristics and operations of TMS-5X processors.				

C03	Understand the functions and operations of TMS-3X processors.
C04	Analyze the performance and characteristics of ADSP.
C05	Compare the performance of various advanced DSP and applications.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	2												
C02	3		2									2	
C03	3		2									2	
C04	3		2		2							3	2
C05	3				3							2	3

23VLE608	PHYSICAL DESIGN OF VLSI CIRCUITS	L	T	P	C	
		3	0	0	3	
COURSE OBJECTIVES :						
<ul style="list-style-type: none"> To Understand the basic concepts of gate array with algorithm paradigms To understand the fundamental routing techniques used in FPGA design 						
UNIT I	INTRODUCTION TO VLSI TECHNOLOGY					9
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms						
UNIT II	PLACEMENT USING TOP-DOWN APPROACH					9
Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic-Ratio cut-partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning-hierarchical approach- simulated annealing- Floor plan sizing. Placement: Cost function- force directed method- placement by simulated annealing-partitioning placement- module placement on a resistive network – regular placement-linear placement.						
UNIT III	ROUTING USING TOP DOWN APPROACH					9
Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches- hierarchical approaches- multi commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming .Detailed Routing: Channel Routing-Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs .						
UNIT IV	PERFORMANCE ISSUES IN CIRCUIT LAYOUT					9
Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization.						
UNIT V	SINGLE LAYER ROUTING CELL GENERATION AND COMPACTION					9
Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.						
		L : 45	T:0	P: 0	Total: 45 PERIODS	
REFERENCES						
1	Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill International Edition 1995.					
2	Preas M. Lorenzatti, “ Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.					

3	Wayne Wolf, "Modern VLSI Design System – On-chip Design", Pearson Education First Indian Reprint 2002.
4	Khosrow Golshan,"Physical Design Essentials: An ASIC Design Implementation Perspective, Springer, 2010

COURSE OUTCOMES

At the end of the course student should be able to:

C01	Understand the basic concepts of gate array with algorithm paradigms
C02	Infer the methods of placement and partitioning using various algorithms
C03	Analyse the fundamental routing techniques used in FPGA design
C04	Estimate various performance metrics in FPGA circuit layout
C05	Familiarize the concepts of circuit compaction in PLA

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	2												
C02	3	2	2	2								3	3
C03	2												
C04	2												
C05	3												

23VLE609	SIGNAL INTEGRITY FOR HIGH SPEED DEVICES	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To Understand the fundamentals of signal integrity for high speed devices To infer the differential signal techniques used in high speed devices 					
UNIT I	SIGNAL INTEGRITY AND ELECTROMAGNETIC WAVE PROPAGATION	9			
The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-max well equations common vector operators-wave propagations-Electro statics- magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves.					
UNIT II	CROSS TALK	9			
Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model.					
UNIT III	DI-ELECTRIC MATERIALS	9			
Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in dielectric behavior Transmission line parameters for loosy dielectric and realistic conductors.					
UNIT IV	DIFFERENTIAL SIGNALING	9			
Removal of common mode noise-Differential Cross talk-Virtual reference plane-propagation of model voltages common terminology-drawbacks of Differential signaling.					
UNIT V	PHYSICAL TRANSMISSION LINE MODEL	9			
Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination.					
		L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES					
1	Advanced Signal Integrity for High-Speed Digital Designs By Stephen H. Hall, Howard L. Heck, 2009.				
2	Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS by James Edgar Buchanan, 1996				
3	Dr. Spartaco Caniggia,"Signal Integrity and Radiated Emission of High-Speed Digital Systems,Wiley,2008				
4	Stephen C. Thierauf,"High-Speed Circuit Board Signal Integrity,Artech House,1st edition,2004				
COURSE OUTCOMES					
At the end of the course student should be able to:					

C01	Understand the fundamentals of signal integrity for high speed devices.
C02	Analyze the crosstalk in inductive and capacitive modeled high speed devices
C03	Estimate the behavior of dielectric materials and its characteristics
C04	Infer the differential signal techniques used in high speed devices
C05	Illustrate the concepts physical transmission model by push-pull transmitter and receivers.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	2												
C02	3	3											
C03	3			3									
C04	3												3
C05	2		3										

23VLE610	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To understand the concepts of active and programmable filters in mixed signal circuits. To Relate the techniques used for analog and mixed signal extensions to verilog 					
UNIT I	VLSI AND ITS ALLIED FIELD	9			
Introduction to Active Filters (PLL) & Switched capacitor filters Active RC Filters for monolithic filter design: First & Second order filter realizations - universal active filter (KHN) - self tuned filter - programmable filters - Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad.					
UNIT II	CONTINUOUS TIME FILTERS& DIGITAL FILTERS	9			
Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors – BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Digital Filters: Sampling – decimation – interpolation - implementation of FIR and IIR filters.					
UNIT III	DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS	9			
Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's.					
UNIT IV	ANALOG AND MIXED SIGNAL EXTENSIONS TO VHDL	9			
Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples.					
UNIT V	ANALOG EXTENSIONS TO VERILOG	9			
Introduction –data types –Expressions-Signals-Analog Behavior-Hierarchical structures-Mixed Signal Interaction. Introduction - Equation construction - solution - waveform Filter functions - simulator - Control Analysis - Multi -disciplinary model.					
		L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES					
1	David A. Johns, Ken Martin, “Analog Integrated Circuit Design” John Wiley & Sons, 2013.				
2	Rudy van de Plassche “Integrated Analog-to-Digital and Digital-to-Analog Converters“, Kluwer 1999.				

3	Antoniou, "Digital Filters Analysis and Design" Tata McGraw Hill, 1998.
4	Phillip Allen and Douglas Holmberg "CMOS Analog Circuit Design" Oxford University.
5	BenhardRazavi, "Data Converters", Kluwer Publishers, 1999
COURSE OUTCOMES	
At the end of the course student should be able to:	
CO1	Understand the concepts of active and programmable filters in mixed signal circuits.
CO2	Familiarize the digital and continuous time filters used in mixed signal circuits.
CO3	Infer the need of ADC/DAC in mixed signal circuits to improve linearity.
CO4	Relate the techniques used for analog and mixed signal extensions to VHDL
CO5	Relate the techniques used for analog and mixed signal extensions to verilog.

Mapping of Programme Outcomes / Programme Specific Outcomes													
(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)													
COs	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
CO1	3	2											
CO2	3												
CO3		3											
CO4				2									
CO5			3	3		3							3

23VLE611	GENETIC ALGORITHMS FOR VLSI	L	T	P	C	
		3	0	0	3	
COURSE OBJECTIVES :						
<ul style="list-style-type: none"> To Understand the fundamentals of genetic algorithm. To Apply Genetic algorithm in VLSI and compare its performance with conventional algorithms. 						
UNIT I	OVERVIEW OF GENETIC ALGORITHMS					9
Introduction to GA Technology - Simple GA algorithm -Steady State Algorithm - Selection - Crossover - Mutation - Fitness Scaling - Inversion.						
UNIT II	GENETIC ALGORITHM FOR VLSI DESIGN					9
GA for VLSI Design, Layout and Test automation - Partitioning - Automatic Placement - Automatic Routing- Technology mapping for FPGAs - Automatic test generation - Genetic Multiway Partitioning.						
UNIT III	ADVANCED GENETIC ALGORITHMS					9
Hybrid genetic - Genetic encoding - Local improvement - WDFR - Comparison of CAs - Standard cell placement - GASP algorithm - Unified algorithm.						
UNIT IV	GENETIC ALGORITHM FOR VLSI TESTING					9
Macro Cell Global routing - FPGA technology mapping - Circuit segmentation - Test generation in a GA frame work - Test generation procedures.						
UNIT V	APPLICATIONS					9
Power estimation - Application of GA - Standard cell placement - GA for ATG - Problem Encoding - Fitness function - GA Vs Conventional Algorithm.						
		L : 45	T:0	P: 0	Total: 45 PERIODS	
REFERENCES						
1	Pinaki Mazumder, E.MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1999					
2	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Second Edition, John Wiley & Sons, 2004					
3	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 2001.					
4	M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley, 1997					
5	John R.Koza, Forrest H.Bennett, David Andre, Morgan Kufmann, "Genetic Programming: Automatic Discovery of Reusable Programs", MIT Press, 1999.					
COURSE OUTCOMES						
At the end of the course student should be able to:						
CO1	Understand the fundamentals of genetic algorithm.					
CO2	Apply genetic algorithm to various stages of VLSI design such as floor planning, partitioning and placement.					
CO3	Analyze various advanced genetic algorithms.					
CO4	Generate optimal vectors for testing, FPGA mapping, automatic test generation and power					

	estimation using genetic algorithm.
C05	Apply Genetic algorithm in VLSI and compare its performance with conventional algorithms.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	2												
C02	3			2	3							2	
C03	3			3	3								
C04	2											2	
C05	3					3							

23VLE612	ADVANCED WIRELESS SENSOR NETWORKS	L	T	P	C	
		3	0	0	3	
COURSE OBJECTIVES :						
<ul style="list-style-type: none"> To Design, analyze and implement different network architectures. To Design and implement simple wireless network concepts. 						
UNIT I	OVERVIEW OF WIRELESS SENSOR NETWORKS					9
Challenges for wireless sensor networks-characteristics requirements-required mechanisms, difference between mobile ad-hoc and sensor networks, applications of sensor networks- case study, enabling technologies for wireless sensor networks.						
UNIT II	ARCHITECTURES					9
Single-node architecture - hardware components, energy consumption of sensor nodes , operating systems and execution environments, network architecture - sensor network scenarios, optimization goals and figures of merit, gateway concepts. Physical layer and transceiver design considerations.						
UNIT III	MAC AND ROUTING					9
DC MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , the mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.						
UNIT IV	INFRASTRUCTURE ESTABLISHMENT					9
Topology control, clustering, time synchronization, localization and positioning, sensor tasking and control.						
UNIT V	DATA MANAGEMENT AND SECURITY					9
Data management in WSN, storage and indexing in sensor networks, query processing in sensor, data aggregation, directed diffusion, tiny aggregation, greedy aggregation, security in WSN, security protocols for sensor networks, secure charging and rewarding scheme, secure event and event boundary detection.						
		L : 45	T:0	P: 0	Total: 45 PERIODS	
REFERENCES						
1	Holger Karl & Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks" , John Wiley, 2007.					
2	Erdal Çayirci , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.					
3	Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks-S Technology, 2010. Protocols, and Applications", John Wiley, 2007.					
4	Erdal Çayirci , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John					

	Wiley and Sons, 2009.
COURSE OUTCOMES	
At the end of the course student should be able to:	
C01	Design and implement simple wireless network concepts.
C02	Analyze and implement different network architectures.
C03	Implement MAC layer and routing protocols.
C04	Deal with timing and control issues in wireless sensor networks.
C05	Develop secured wireless sensor networks.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3		2	2	2	2	2					1	2
C02	3	2	3	2	2						2	2	2
C03	3	2	3	2	2		2			2		2	2
C04	2	3	2	2	2	3	2		2			2	2
C05	2	2	3	2	2	3	2		2			3	1

PROFESSIONAL ELECTIVE III

23VLE613	VLSI ARCHITECTURE FOR IMAGE AND VIDEO PROCESSING	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> • To analyze the Image and Video processing algorithms. • To explore various processing techniques of Image and Video signals. 					
UNIT I	IMAGE PROCESSING ALGORITHMS	9			
Introduction – Image Processing Tasks- Low level Image Processing Operations – Description of some intermediate level operations –Requirements for Image processor architecture					
UNIT II	IMAGE PROCESSING ARCHITECTURES AND PIPELINED LOW LEVEL IMAGE PROCESSING	9			
Classification of Architectures – Uni and Multi processors – MIMD systems – SIMD systems – Pipelines – Devices for cellular logic processing – Design aspects of real time low level image processors –Design method for special architectures.					
UNIT III	PIPELINED ARCHITECTURES & 2D AND 3D IMAGE PROCESSING ARCHITECTURES	9			
Architecture of a cellular logic processing element – Second decomposition in data path and control – Real time pipeline for low level image processing – Design aspects of Image Processing architectures – Implementation of Low level 2D and 3D and Intermediate level algorithms.					
UNIT IV	VIDEO PROCESSING ALGORITHMS	9			
Motion Estimation Algorithms – Complexity Analysis Methodology –Complexity analysis of MPEG – 4 Visual – Analysis of Fast Motion Estimation Algorithms.					
UNIT V	VLSI ARCHITECTURES FOR VIDEO PROCESSING	9			
General design space evaluation – Design space motion estimation architectures – Motion estimation architectures for MPEG-4 – Design Tradeoffs – VLSI Implementation search engine I and Search engine II.					
L : 45		T:0	P: 0	Total: 45 PERIODS	
REFERENCES					
1	Peter M. Kuhn, –Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation ", Springer ISBN 978-1-4419-5088-8, First Edition, 2010.				
2	Pieter Jonker, –Morphological Image Processing: Architecture and VLSI design , Springer. ISBN: 9020127667, First Edition, 1992.				
3	Rafael C. Gonzalez & Richard E. Woods, -Digital Image Processing , Prentice Hall; Third edition, 2008.				
4	A.MuratTekalp, –Digital Video Processing , Pearson Education, Noida, First Edition, 2010.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Analyze the algorithms and operations of VLSI image processors.				
CO2	Classify the types of image processing architectures and its design methodologies.				

C03	Infer the functions of pipelined, 2D and 3D algorithms in image processors
C04	Estimate the complexity of video processing by motion estimation algorithms.
C05	Understand the design tradeoff of videos using VLSI architecture

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01		3	3	3	3	3						2	
C02	3				3								
C03	3				3								
C04		3											
C05	3					3	3					2	

23VLE614	NETWORK ON CHIP				L	T	P	C
		3	0	0	3			
COURSE OBJECTIVES :								
<ul style="list-style-type: none"> To Understand the concept of network on chip To Learn router architecture designs 								
UNIT I	INTRODUCTION TO NOC							9
Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality of-Service Support								
UNIT II	ARCHITECTURE DESIGN							9
Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design								
UNIT III	ROUTING ALGORITHM							9
Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms								
UNIT IV	TEST AND FAULT TOLERANCE OF NOC							9
Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips.								
UNIT V	THREE DIMENSIONAL INTEGRATION OF NETWORK ON CHIP							9
Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks On-Chip.								
		L : 45	T:0	P: 0	Total: 45 PERIODS			
REFERENCES								
1	ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das” Networks-On - Chip “ Architectures Holistic Design Exploration”, Springer.							
2	Fayezgeballi, Haythamelmiligi, Hqhahedwatheq E1-Kharashi “Networks-On-Chips Theory and Practice CRC Press							
3	Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013							
4	Palesi, Maurizio, Daneshtalab, Masoud “Routing Algorithms in Networks-On-Chip” 2014							
5	Santanu Kundu, Santanu Chattopadhyay “Network-on-Chip: The Next Generation of System on-Chip Integration”, CRC Press, 2014							
COURSE OUTCOMES								
At the end of the course student should be able to:								
CO1	Compare different architecture design							
CO2	Discuss different routing algorithms							

C03	Explain three dimensional Networks on Chip architectures
C04	Test and design fault tolerant NOC
C05	Design three dimensional architectures of NOC

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3				3								
C02	3				3								
C03	3				3								
C04		3	3	3									
C05		3	3	3					3	2		3	3

23VLE615	CAD FOR VLSI DESIGN				L	T	P	C
		3	0	0	3			
COURSE OBJECTIVES :								
<ul style="list-style-type: none"> To Introduce the VLSI design methodologies and design methods. . To Learn data structures and algorithms required for VLSI design. 								
UNIT I	INTRODUCTION							9
Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools.								
UNIT II	DATA STRUCTURES AND BASIC ALGORITHMS							9
Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.								
UNIT III	ALGORITHMS FOR PARTITIONING AND PLACEMENT							9
Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.								
UNIT IV	ALGORITHMS FOR FLOORPLANNING AND ROUTING							9
Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.								
UNIT V	MODELLING, SIMULATION AND SYNTHESIS							9
Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.								
		L : 45	T:0	P: 0	Total: 45 PERIODS			
REFERENCES								
1	Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.							
2	Naveed a. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3 rd Edition, Springer, 2017.							
3	Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1 st Edition, 2019.							
4	N.a. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.							
5	Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.							
COURSE OUTCOMES								
At the end of the course student should be able to:								
CO1	Use various VLSI design methodologies							
CO2	Infer the techniques used to design adders and multipliers architectures.							
CO3	Analyze and synthesis the low power VLSI circuits of various levels of abstraction							
CO4	Examine the banked organization of low power static RAM architectures							
CO5	Model a low power circuits with energy recovery techniques.							

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3			3								3	
C02	3			3									
C03		3	3										
C04		2											
C05		2	2		3				3			3	

23VLE616	NANOSCALE DEVICES			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES :							
<ul style="list-style-type: none"> To Understand the fundamentals of mesoscopic electron transport and the influence of dimensionality of the object at nanoscale on their properties. To learn the concept of mesoscopic super conductivity and solid state qubits. 							
UNIT I	FUNDAMENTALS OF MESOSCOPIC ELECTRON TRANSPORT						9
Review of classical transport, Coherent and ballistic transport, Tunneling, Landauer-Buttiker formalism, 2D and 1D transport, Conductance quantization, Aharonov-Bohm effect, Weak localization and conductance fluctuations, Mesoscopic noise							
UNIT II	CHARGING EFFECTS AND SINGLE ELECTRONICS						9
Introduction, Coulomb blockade, Single-electron box, single-electron transistor, RF-SET, Orthodox theory.							
UNIT III	LOW DIMENSIONAL SYSTEMS						9
Introduction, 2D electron gas, Quantum Hall effect, Nanowires, nanotubes and 1D transport, Quantum point contacts, quantum dots.							
UNIT IV	MESOSCOPIC SUPERCONDUCTIVITY						9
Superconducting basics, Cooper-pairs and quasiparticles, Josephson junctions, Flux quantization and SQUIDS, single-cooper box.							
UNIT V	SOLID-STATE QUBITS						9
Superconducting qubits, Semiconductor qubits, Circuit quantum electrodynamics.							
L : 45				T:0	P: 0	Total: 45 PERIODS	
REFERENCES							
1	Electronic Transport in Mesoscopic Systems, Supriyo Datta, Cambridge University Press (1997)						
2	Quantum transport, Y. V. Nazarov et Y. M. Blanter. Cambridge University Press, (2009).						
3	Sandip Tiwari, "Nanoscale Device Physics" Oxford University Press; 1st edition (2017)						
4	Brajesh Kumar Kaushik, "Nanoscale Devices: Physics, Modeling, and Their Application", CRC Press; 1st edition, 2018						
COURSE OUTCOMES							
At the end of the course student should be able to:							
CO1	Understand the fundamental principles governing mesoscopic electron transport phenomena.						
CO2	Comprehend charging effects in mesoscopic systems.						
CO3	Ability to understand Low dimensional systems of Nanoscale devices.						
CO4	Analyze the behavior of Josephson junctions and demonstrate proficiency in understanding their applications in mesoscopic circuits.						
CO5	Apply Concepts in Quantum Computing						

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3											2	
C02		3	3	2								2	
C03	3	3	3									2	
C04		3	3	2								2	
C05		3	3	2								2	

23VLE617	VLSI FOR WIRELESS COMMUNICATION	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To learn the concepts of basic wireless communication concepts. To discuss the circuits such as low noise amplifiers, mixers, power amplifiers, oscillators and phase locked loops 					
UNIT I	COMMUNICATION CONCEPTS	9			
Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Standard Translation.					
UNIT II	RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS	9			
Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.					
UNIT III	MIXERS	9			
Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.					
UNIT IV	FREQUENCY SYNTHESIZERS	9			
PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider.					
UNIT V	TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS	9			
Transmitter back end design – Quadrature LO generator – Power amplifier design.					
L : 45		T:0	P: 0	Total: 45 PERIODS	
REFERENCES					
1	Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2014.				
2	B.Razavi , “RF Microelectronics” , Prentice-Hall ,2 nd Edition, 2011.				
3	Behzad Razavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 2000.				
4	Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI wireless design – Circuits & Systems”, Kluwer Academic Publishers, 2000.				
5	Thomas H.Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Cambridge University Press ,2003.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
C01	Understand the concepts of basic wireless communication concepts.				
C02	Study the parameters in receiver and low noise amplifier design.				
C03	Analyse the various types of mixers designed for wireless communication.				
C04	Design PLL and VCO.				
C05	Illustrate the concepts of transmitters and power amplifiers in wireless communication.				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	PS01	PS02
C01	3			3						3			3
C02	3			2									
C03	3			3									
C04	3	3	3										3
C05	3			3					3				3

23VLE618	POWER EFFICIENT VLSI DESIGN	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES :					
<ul style="list-style-type: none"> To understand the different leakage power reduction techniques To design low voltage CMOS circuits to reduce power consumption and low energy circuits 					
UNIT I	POWER DISSIPATION IN CMOS	9			
Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.					
UNIT II	POWER OPTIMIZATION	9			
Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design – Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design					
UNIT III	DESIGN OF LOW POWER CMOS CIRCUITS	9			
Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.					
UNIT IV	POWER ESTIMATION	9			
Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis – Probabilistic Power Analysis.					
UNIT V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS	9			
Synthesis for Low Power – Behavioral Level Transform – Algorithms for Low Power – Software Design for Low Power.					
		L : 45	T:0	P: 0	Total: 45 PERIODS
REFERENCES					
1	Kaushik Roy and S.C.Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2009				
2	J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 2007.				
3	James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001				
4	Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009.				
COURSE OUTCOMES					
At the end of the course student should be able to:					
CO1	Infer the basic concepts of power dissipation in Low power VLSI circuits.				
CO2	Design and analyze various MOS logic circuits.				
CO3	Apply low power techniques for low power dissipation.				
CO4	Estimate the power dissipation of ICs.				
CO5	Develop algorithms to reduce power dissipation by software tools				

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
C01	3			3								3	
C02		3	3	3	3								
C03		3	3	3								3	
C04		3	3	3	3		3		3			3	3
C05		3	3	3	3		3		3			3	3

PROFESSIONAL ELECTIVE IV

23VLE619	SYSTEM VERILOG			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To provide a comprehensive understanding of System Verilog, including its syntax, data structures, and control constructs To equip with the knowledge and skills to address hardware security challenges 							
UNIT I	BASICS OF SYSTEM VERILOG						9
Basic blocks of computers – Algorithm, Pseudo code, Flowchart - Structure of C program- Data Introduction to System Verilog – Packages – Declarations – Simulation Time Units – Precision – Variables – Data Types.							
UNIT II	DATA STRUCTURES						9
Structures – Declarations – Packed Structures – Passing Structures – Unions – Packed, unpacked, Tagged Unions - Arrays – Array Operation							
UNIT III	STATEMENTS AND CONTROL STRUCTURES						9
Procedural Blocks – Combinational, Sequential and Latched Logic – Enhancements to Tasks and Functions – Operand Enhancements – New Jump Statements – Enhanced Case Statements – Enhanced if else Decision							
UNIT IV	SYSTEM VERILOG DESIGN VERIFICATION						9
Verification method implementation – Response checking – Assertions – Internal DUT signals- External interfaces – Reusable assertions based checkers							
UNIT V	HARDWARE SECURITY						9
Reasons for raise of hardware security issues – IC Counterfeiting – IP piracy – Hardware Trojans – Debug security and applications of Physical Unclonable Functions (PUF)							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Janick Bergeron, “Writing Test Benches Functional Verification of HDL Models”,3 rd edition,Springer, 2003						
R2	Andreas Meyer, “Principles of Functional Verification”, 5 th edition, Newness, 2003.						
R3	Chris Spear, “System Verilog for Verification: A Guide to Learning the Test benchLanguage Features”, 3 rd edition, Springer, 2012.						
R4	T.Kropf, “Introduction to Formal Hardware Verification”, 7 th edition, Springer Verlag, 2010.						
R5	Stuart Sutherland, Simon Davidmann, and Peter Flake”SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling”,Springer,2nd Edition,2006						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Explain the basic concepts of System Verilog.						
CO 2	Illustrate the operations of data structures						
CO 3	Make use of procedural statements in system Verilog programming.						

CO 4	Summarize different verification process in system Verilog.
CO 5	Analyze security issues in hardware using system Verilog

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3												
CO2	3												
CO3	3												
CO4	3	3	3		3		3		3			3	
CO5	3	3			3				3	3		2	3

23VLE620	HARDWARE SOFTWARE CO-DESIGN FOR FPGA			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To understand the principles of hardware/software co-design, system specification, and modeling techniques for embedded systems. To equip with the skills to perform hardware/software partitioning, co-synthesis, and system-level design verification 							
UNIT I	SYSTEM SPECIFICATION AND MODELLING						9
Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification							
UNIT II	HARDWARE/SOFTWARE PARTITIONING						9
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.							
UNIT III	HARDWARE/SOFTWARE CO-SYNTHESIS						9
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.							
UNIT IV	PROTOTYPING AND EMULATION						9
Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.							
UNIT V	DESIGN SPECIFICATION AND VERIFICATION						9
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation, A Case Study on Hardware/Software Codesign in Embedded Artificial Neural Networks.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer, 2010.						
R2	Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Publisher, 2010.						
R3	Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Publisher, 2007.						
R4	Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publisher, 2001.						
R5	Joao Cardoso and Michael Hübner "Reconfigurable Computing: From FPGAs to						

23VLE621	ADAPTIVE SIGNAL PROCESSING			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To understand the fundamental concepts of discrete random signal processing To develop expertise in spectral estimation and adaptive filtering techniques 							
UNIT I	DISCRETE RANDOM SIGNAL PROCESSING						9
Discrete Random Processes, Random Variables, Parseval's Theorem, Wiener-Khintchine Relation, Power Spectral Density, Spectral Factorization, Filtering Random Processes, Special Types of Random Processes.							
UNIT II	SPECTRAL ESTIMATION						9
Introduction, Nonparametric Methods – Periodogram, Modified Periodogram, Bartlett, Welch and Blackman-Tukey Methods, Parametric Methods – ARMA, AR and MA Model Based Spectral Estimation, Solution Using Levinson-Durbin Algorithm							
UNIT III	WEINER AND ADAPTIVE FILTERS						9
Weiner Filter: FIR Wiener Filter, IIR Wiener Filter, Adaptive Filter: FIR Adaptive Filters – Steepest Descent Method- LMS Algorithm, RLS Adaptive Algorithm, Applications.							
UNIT IV	DETECTION AND ESTIMATION						9
Bayes Detection Techniques, Map, ML,– Detection of M-Ary Signals, Neymanpearson, Minimax Decision Criteria. Kalman Filter- Discrete Kalman Filter, The Extended Kalman Filter, Application.							
UNIT V	SYNCHRONIZATION						9
Signal Parameter Estimation, Carrier Phase Estimation, Symbol Timing Estimator, Joint Estimation of Carrier Phase and Symbol Timing							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Bernard Widrow and Samuel D. Stearns, “adaptive signal processing” , 1 st Edition Pearson publication, 2002.						
R2	Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2009						
R3	John G. Proakis., “Digital Communication”, 4 th Edition, McGraw Hill Publications, 2001.						
R4	Simon Haykin, “Adaptive Filter Theory”, Pearson Education, Fourth Edition, 2003.						
R5	Aurelio Uncini”Fundamentals of Adaptive Signal Processing”,Springer,1st Edition,2014						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Analyze the basic principles of discrete random signal processing .						
CO 2	Analyze the principles of spectral estimation.						
CO 3	Analyze the Weiner and Adaptive filters						
CO 4	Analyze the different signal detection and estimation methods.						
CO 5	Design the synchronization methods for proper functioning of the system.						

COs	Mapping of Programme Outcomes / Programme Specific Outcomes (1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3												
CO2	3												
CO3	3			3									
CO4		3		3									
CO5		3	3		3		3						

23VLE622	DESIGN OF SEMICONDUCTOR MEMORIES	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES:					
<ul style="list-style-type: none"> To provide a comprehensive understanding of memory technologies and architectures To develop the ability to analyze and address challenges in memory systems 					
UNIT I	RANDOM ACCESS MEMORY TECHNOLOGIES	9			
SRAM cell structures - MOS SRAM architectures, MOS SRAM cell, Bipolar SRAM technologies, Silicon On Insulator (SOI) technology, advanced SRAM architectures and technologies. DRAM technology development - CMOS DRAMs, DRAMs cell theory, Bi-CMOS, DRAMs, soft error failures in DRAMs, advanced DRAM designs and architectures					
UNIT II	NON-VOLATILE MEMORIES	9			
Masked Read-Only Memories - High density ROMs. Programmable Read-Only Memories - Bipolar PROMs, CMOS PROMs. EPROMs - Floating-Gate EPROM Cell, One-Time Programmable EEPROMs - EEPROM technology and architectures, non-volatile SRAM,Flash memories (EPROMs or EEPROM) - advanced flash memory architectures.					
UNIT III	MEMORY FAULT MODELING AND TESTING	9			
RAM fault modeling - Electrical testing - Pseudo random testing - Megabit DRAM testing non-volatile memory modeling and testing - IDDQ fault modeling and testing - Application specific memory testing					
UNIT IV	SEMICONDUCTOR RADIATION EFFECTS	9			
Radiation effects - Single event phenomenon - Radiation hardening techniques - Radiation hardening process and design issues – Radiation hardened memory characteristics - Radiation hardness assurance and testing - Radiation dosimetry - Water level radiation testing and test structures					
UNIT V	ADVANCED MEMORY TECHNOLOGIES	9			
Introduction to memory technologies - High-density memory packing technologies - Gallium Arsenide (GaAs) FRAMs - Analog Memories - Magneto Resistive Random Access Memories - Experimental Memory Devices. Ferroelectric Random Access Memories - Memory hybrids and MCMs (2D) - Memory stacks and MCMs (3D).					
		L:45	T:0	P: 0	Total: 45 Periods
REFERENCES					
R1	Ashok.K.Sharma, “Semiconductor Memories: Technology, Testing and Reliability”, Wiley IEEEpress, New York, 2 nd Edition,2010.				
R2	Brent Keeth, R. Jacob Baker, Brian Johnson, Freng Lin, “DRAM Circuit Design: Fundamental and High Speed Topics”, Wiley-IEEE Press, 2 nd edition, 2012.				
R3	Andrea Redaelli and Fabio Pellizzer,“Semiconductor Memories and Systems,Elsevier,1st Edition,2022				
R4	Betty Prince,“Semiconductor Memories: A Handbook of Design, Manufacture and Application,Wiley,2nd Edition”,1996				
R5	Shimeng Yu,“Semiconductor Memory Devices and Circuits”,CRC Press,1st Edition,2022				
COURSE OUTCOMES					
At the end of the course students should be able to					
CO 1	Illustrate the micro level operations of Random Access Memories.				

CO 2	Compare the performance of various non-volatile memories.
CO 3	Identify the suitable fault modeling technique for memory testing.
CO 4	Outline the radiation effects of memory.
CO 5	Summarize the concepts of advanced memory technologies.

COs	Mapping of Programme Outcomes / Programme Specific Outcomes (1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3												
CO2	3												
CO3		3	3										
CO4	3												
CO5	3			3					3				

23VLE623	SOLAR PHOTO VOLTAIC SYSTEM			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To impart foundational knowledge of photovoltaic systems and their components To develop the ability to design and analyze photovoltaic and hybrid energy systems 							
UNIT I	PHOTOVOLTAIC BASICS						9
Structure and working of Solar Cells - Types, Electrical properties and Behaviour of Solar Cells – Cell properties and design - PV Cell Interconnection and Module Fabrication - PV Modules and arrays - Basics of Load Estimation.							
UNIT II	STAND ALONE PV SYSTEMS						9
Schematics, Components, Batteries, Charge Conditioners - Balance of system components for DCand/or AC Applications - Typical applications for lighting, water pumping etc.							
UNIT III	GRID CONNECTED PV SYSTEMS						9
Schematics, Components, Charge Conditioners, Interface Components - Balance of system Components - PV System in Buildings.							
UNIT IV	HYBRID SYSTEMS						9
Solar, Biomass, Wind, Diesel Hybrid systems - Comparison and selection criteria for a given application.							
UNIT V	DESIGN OF PV SYSTEMS						9
Radiation and load data - Design of System Components for different PV Applications - Sizing and Reliability - Simple Case Studies.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Angèle Reinders, Pierre Verlinden, Wilfried van Sark, and Alexandre Freundlich,"Photovoltaic Solar Energy: From Fundamentals to Applications,Wiley,1st Edition,2017						
R2	Adel Mellit, Mohamed Benghanem, and Ahmad Taher Azooz,"Photovoltaic Systems: Fundamentals and Applications,Photovoltaic Systems: Fundamentals and Applications,Springer,1st Edition,2022						
R3	Jay Warmke,"Designing & Installing Solar PV Systems,Solar Energy International Description,2nd Edition,2022						
R4	Michael Boxwell,"Solar Electricity Handbook,Greenstream Publishing Description,Greenstream Publishing Description,2023						
R5	Antonio Luque and Steven Hegedus,"Handbook of Photovoltaic Science and Engineering,Wiley Description,2nd Edition,2011						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Explain basics of solar photovoltaic systems basics.						
CO 2	Understand the basics of solar photovoltaic systems.						
CO 3	Know in depth of its types and design of various PV-interconnected systems.						
CO 4	Outline the importance of hybrid systems.						

CO 5	Summarize the concepts of design of PV Systems.
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COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3												
CO2	3												
CO3	3			3									
CO4	3			3									
CO5	3			3					3				

PROFESSIONAL ELECTIVE V

23VLE624	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES:					
<ul style="list-style-type: none"> ● To understand the principles and technologies of DSP integrated circuits and VLSI design ● To develop expertise in the design and implementation of DSP algorithms and architectures 					
UNIT I	DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES	9			
Standard Digital Signal Processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.					
UNIT II	DIGITAL SIGNAL PROCESSING	9			
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.					
UNIT III	DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS	9			
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects.					
UNIT IV	SYNTHESIS OF DSP ARCHITECTURES	9			
Multiprocessors and multicomputer, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.					
UNIT V	ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN	9			
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.					
L:45		T:0	P: 0	Total: 45 Periods	
REFERENCES					
R1	A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2009.				
R2	Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Pearson Education, Asia, 2009.				
R3	KeshabK.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.				
R4	Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 2014.				
R5	Peter Pirsch"Architectures for Digital Signal Processing"Wiley,2009				
COURSE OUTCOMES					
At the end of the course students should be able to					
CO 1	Understand the technologies used to design standard DSP processors.				
CO 2	Identify the frequency response of DSP by types of Fourier transforms.				

23VLE625	MIXED SIGNAL VLSI DESIGN	L	T	P	C
		3	0	0	3
COURSE OBJECTIVES:					
<ul style="list-style-type: none"> To provide a comprehensive understanding of advanced circuit techniques in mixed-signal design To develop expertise in data conversion techniques for signal processing 					
UNIT I	SWITCHED CAPACITOR CIRCUITS	9			
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.					
UNIT II	PHASED LOCK LOOP (PLL)	9			
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications					
UNIT III	DATA CONVERTER FUNDAMENTALS	9			
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.					
UNIT IV	NYQUIST RATE A/D CONVERTERS	9			
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters					
UNIT V	OVERSAMPLING CONVERTERS	9			
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.					
		L:45	T:0	P: 0	Total: 45 Periods
REFERENCES					
R1	Shirshendu Roy,"Advanced Digital System Design A Practical Guide to Verilog Based FPGA and ASIC Implementation",Springer Cham,1st Edition,2024				
R2	Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning ,7 th edition,2013.				
R3	John.F.Wakerly,"Digital Design: Principles and Practices",4th Edition,Pearson,2008.				
R4	Parag K.Lala "Digital system Design using PLD" B S Publications,2003.				
COURSE OUTCOMES					
At the end of the course students should be able to					
CO 1	Analyze and design switched capacitor circuits				
CO 2	Understand and apply phase-locked loop (PLL) concepts				
CO 3	Designing data converters and know how to use these in specific applications.				
CO 4	Design and analyze Nyquist rate A/D converters:				
CO 5	Apply oversampling techniques in data converters				

23VLE626	RECONFIGURABLE ARCHITECTURES			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To provide a comprehensive understanding of reconfigurable computing systems and their applications To develop skills in design, management, and application of reconfigurable systems 							
UNIT I	INTRODUCTION						9
General purpose computing – domain specific processors – Application Specific Processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse grained reconfigurable devices.							
UNIT II	IMPLEMENTATION, SYNTHESIS AND PLACEMENT						9
Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device’s free and occupied spaces							
UNIT III	COMMUNICATION AND SOPC						9
Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.							
UNIT IV	RECONFIGURATION MANAGEMENT						9
Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.							
UNIT V	APPLICATIONS						9
FPGA based parallel pattern matching - low power FPGA based architecture for microphone arrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer 2007.						
R2	Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA Based Computation”, Elsevier 2008.						
R3	M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2010.						
R4	Nikoloas Voros Et Al. “Applied Reconfigurable Computing: Architectures, Tools and Applications” Springer, 2018.						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Analyze the different architecture principles relevant to reconfigurable computing systems.						
CO 2	Compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems.						

23VLE627	DESIGN FOR VERIFICATION USING UVM			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To understand the principles and architecture of Universal Verification Methodology (UVM) To develop expertise in implementing and managing UVM-based verification environments 							
UNIT I	INTRODUCTION						9
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation.							
UNIT II	DEVELOPING REUSABLE VERIFICATION COMPONENTS						9
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation - Managing of Test-Implementing Checks and Coverage.							
UNIT III	UVM USING VERIFICATION COMPONENTS						9
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards Implementing a Coverage Module.							
UNIT IV	UVM USING THE REGISTER LAYER CLASSES						9
Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register-Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences.							
UNIT V	ASSIGNMENT IN TESTBENCHES						9
Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi, 2013.						
R2	SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2012.						
R3	http://www.testbench.in/ut_00_index.html 3 .						
R4	http://www.testbench.in/ot_00_index.htm						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Understand the basic concepts of two methodologies UVM.						
CO 2	Build actual verification components.						
CO 3	Generate the register layer classes						
CO 4	Code testbenches using UVM.						
CO 5	Understand advanced peripheral bus testbenches						

23VLE628	SOFTCOMPUTING AND OPTIMIZATION TECHNIQUES			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To provide a solid foundation in computational intelligence techniques To develop expertise in hybrid modeling and optimization strategies 							
UNIT I	FUZZY LOGIC						9
Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets- Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.							
UNIT II	ARTIFICIAL NEURAL NETWORKS						9
Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Backpropagation networks: architecture, multilayer perceptron, backpropagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network, Convolutional neural networks. Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.							
UNIT III	GENETIC ALGORITHM						9
Genetic algorithm- Introduction - biological background - traditional optimization and search techniques - Genetic basic concepts - operators - Encoding scheme - Fitness evaluation - crossover - mutation - Travelling Salesman Problem, Particle swarm optimization, Ant colony optimization.							
UNIT IV	NEURO-FUZZY MODELING						9
Adaptive Neuro-Fuzzy Inference Systems (ANFIS) - architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks - Data Clustering Algorithms - Rule base Structure Identification - Neuro-Fuzzy Control - the inverted pendulum system.							
UNIT V	CONVENTIONAL OPTIMIZATION TECHNIQUES						9
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization -sequential linear programming, Interior penalty function method, external penalty function method.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson Education 2015.						
R2	David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.						
R3	Saroj Kaushik Sunita Tewari, "Softcomputing fundamentals" McGraw Hill India, 1st edition 2018.						
R4	Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.						
COURSE OUTCOMES							
At the end of the course students should be able to							

CO 1	Develop application on different soft computing techniques like Fuzzy, GA and Neural network
CO 2	Implement Neuro-Fuzzy and Neuro-Fuzz-GA expert system.
CO 3	Implement machine learning through Neural networks
CO 4	Model Neuro Fuzzy system for clustering and classification.
CO 5	Apply the optimization techniques to solve the real world problems

COs	Mapping of Programme Outcomes / Programme Specific Outcomes												
	(1/2/3 indicates Correlation Levels) 1- Slight(Low) 2- Moderate (Medium) 3-Substantial (High)												
	CO-PO Mapping											CO-PSO Mapping	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3												
CO2		3	3										
CO3		3	3										
CO4		3	3										
CO5		3	3		3		3				3	2	2

OPEN ELECTIVE OFFERED TO OTHER PROGRAMMES

23VLO701	SYSTEM ON CHIP			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> ● To understand the concepts, methodologies, and challenges of System-on-Chip (SoC) design ● To develop skills in validation and testing of SoC design 							
UNIT I	INTRODUCTION						9
System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.							
UNIT II	DESIGN METHODOLOGICAL FOR LOGIC CORES						9
SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores –Designing with hard cores, soft cores- Core and SoC design examples							
UNIT III	DESIGN METHODOLOGY FOR MEMORY AND ANALOG CORES						9
Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase-located loops –High I/O.							
UNIT IV	DESIGN VALIDATION						9
Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip.							
UNIT V	SOC TESTING						9
SoC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories. Case Study: Integrating BIST techniques for on-line SoC testing.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Rochit Rajsunah, System-on-a-chip: Design and Test, Artech House, 2007.						
R2	Prakash Raslinkar, Peter Paterson & Leena Singh, System-on-a-chip verification: Methodology and Techniques, Kluwer Academic Publishers, 2007.						
R3	M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems, Springer, 2007.						
R4	Joseph Yiu, "System-on-Chip Design with Arm® Cortex®-M, Arm education, 2019						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Illustrate the concepts of System on Chip Design methodology						
CO 2	Understand the concepts of for Logic and Analog Cores.						
CO 3	Know the concepts of System on Chip Design Validation.						
CO 4	Perform SoC validation and verification						
CO 5	Apply advanced testing techniques for SoC reliability						

23VLO702	VLSI DESIGN TECHNIQUES			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To provide foundational knowledge of MOS transistor theory and CMOS technology To develop skills in designing and analyzing VLSI circuits and systems 							
UNIT I	MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY						9
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. Basic CMOS technology.							
UNIT II	INVERTERS CIRCUIT ANALYSIS						9
NMOS Inverters, Stick diagram, Inverter ratio, DC characteristics, Transient characteristics , Switching times, Super buffers, Driving large capacitance loads.							
UNIT III	CMOS LOGIC GATES						9
CMOS Inverters, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design.							
UNIT IV	CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION						9
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation, Charge sharing.							
UNIT V	VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN						9
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits– Ripple carry adders, Carry look ahead adders, Multipliers, Physical design – Delay modeling, floor planning.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.						
R2	Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 2002.						
R3	Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2002.						
R4	Stephen Brown,Zvonko Vranesic,"Fundamentals of Digital Logic Design With VHDL",Second Edition 2007.						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Understand the basic concepts of MOS transistor theory and its process technology.						
CO 2	Analyze the CMOS inverter transient and switching characteristics						
CO 3	Infer the types of CMOS digital logic circuits to design a static and dynamic logic design.						
CO 4	Estimate the power dissipation and low power performance of VLSI circuits						
CO 5	Model a system component of VLSI circuits in physical layer of abstraction						

23VLO703	VLSI TECHNOLOGY			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To understand the foundational processes in VLSI fabrication To develop expertise in advanced VLSI process integration and packaging 							
UNIT I	CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION						9
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.							
UNIT II	LITHOGRAPHY AND REACTIVE PLASMA ETCHING						9
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Nano imprint Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipments.							
UNIT III	DEPOSITION, DIFFUSION AND ION IMPLANTATION						9
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick's one dimensional Diffusion Equation - Measurement techniques - Range theory- Implant equipment - Annealing- Shallow junction, High - energy implantation.							
UNIT IV	METALLIZATION AND VLSI PROCESS INTEGRATION						9
Physical Vapour Deposition (PVD) -Patterning- NMOS IC Technology - CMOS IC Technology - BICMOS IC Technology- MOS Memory IC technology - Bipolar IC Technology -Silicon on Insulator Technology-Noise in VLSI Technologies.							
UNIT V	ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES						9
Analytical Beams - Beams Specimen interactions - Chemical methods - Package types - packaging design consideration - VLSI assembly technology - Package fabrication technology.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	S.M .Sze, VLSI Technology, McGraw Hill, 2003..						
R2	James D Plummer, Michael D. Deal and Peter B. Griffin, Silicon VLSI Technology: Wai Kai Chen, VLSI Technology, CRC press, 2003.						
R3	Rainer Waser, Nano Electronics and Information Technology, Wiley VCH - April 2003.						
R4	Neil H. E. Weste, Kamran Eshraghian,"Principles of CMOS VLSI Design",Addison-Wesley,,2010						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Analyze the concepts of Fabrication of ICs and purification of Silicon in different technologies.						
CO 2	Impart in-depth knowledge about Etching and deposition of different layers.						
CO 3	Understand the different packaging techniques of VLSI devices.						
CO 4	Able to understand and integrate new knowledge within the field.						
CO 5	Able to apply advanced technical knowledge in multiple contexts.						

23VLO704	MEMS AND ITS APPLICATIONS			L	T	P	C
				3	0	0	3
COURSE OBJECTIVES:							
<ul style="list-style-type: none"> To impart knowledge of MEMS and microsystem fundamentals To familiarize students with microsystem fabrication techniques 							
UNIT I	MEMS AND MICROSYSTEMS						9
MEMS and Microsystems products, evaluation of micro fabrication, micro-systems and microelectronics, applications of Microsystems, working principles of Microsystems, micro-sensors, micro-actuators, MEMS and micro-actuators, micro-accelerometers. Scaling Laws In Miniaturization: Introduction, scaling in geometry, scaling in rigid body dynamics, the trimmer force scaling vector, scaling in electrostatic forces.							
UNIT II	MATERIALS FOR MEMS						9
Substrates and wafers, silicon as a substrate material, ideal substrates for MEMS, single crystal silicon and wafers crystal structure, mechanical properties of Si, silicon compounds, SiO ₂ , SiC, Si ₃ N ₄ . And polycrystalline Silicon, silicon piezo resistors, gallium arsenide, quartz, piezoelectric crystals, polymers for MEMS, conductive polymers.							
UNIT III	ENGINEERING MECHANICS FOR MICROSYSTEMS DESIGN						9
Introduction, static bending of thin plates, circular plates with edge fixed rectangular plate with all edges fixed and square plates with all edges fixed. Mechanical vibration, resonant vibration, micro accelerometers, design theory and damping coefficients. Thermo mechanics, thermal stresses. Fracture mechanics, stress intensity factors, fracture toughness and interfacial fracture machine.							
UNIT IV	BASICS OF FLUID MECHANICS IN MACRO AND MESO SCALES						9
Viscosity of fluids, flow patterns Reynolds number. Basic equation in continuum fluid dynamics, laminar fluid flow in circular conduits, computational fluid dynamics, and incompressible fluid flow in micro conducts surface tension, capillary effect and micro pumping. Fluid flow in sub micrometer and nanoscale, rare field gas, Knudsen and Mach number and modeling of micro gas flow, heat conduction in multilayered thin films.							
UNIT V	MICROSYSTEM FABRICATION PROCESS						9
Photolithography, photo resist and applications, light sources. Ion implantation, diffusion process, oxidation, thermal oxidation, silicon diode, thermal oxidation rates, Oxide thickness by colour. Chemical vapour deposition, reactants CVD, enhanced CVD physical vapour defusing, sputtering, deposition by epitaxial etching, chemical and plasma etching.							
				L:45	T:0	P: 0	Total: 45 Periods
REFERENCES							
R1	Tai-Ran Hus, MEMS and Microsystems Design and Manufacture, Tata McGraw-Hill, 2017.						
R2	John A Pelesko, Modeling MEMs and NEMS, CRC Press, 2002.						
R3	Chang Liu, Foundation of MEMS, Pearson Edition, 2011						
R4	Stephen Beeby, Graham Ensell, MEMS, Mechanical Sensors, Artech House Publishers, 2004.						
COURSE OUTCOMES							
At the end of the course students should be able to							
CO 1	Understand the fundamental concepts and working principles of MEMS and Microsystems.						
CO 2	Infer the types of material used to design MEMS and microsystem devices.						

